The Computer Conservation Society

EDSAC Replica Project Hardware Note

Number: HN5	Title: **Experiments on Regeneration Chassis**		
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While the original Regeneration Chassis belonging to the University Computer Lab was in our safekeeping it was considered valuable to see how the circuits worked in practice, taking into account the absolute need to cause no damage to the chassis. We have already constructed a replica AND-gate and an Inverter, driven from a modern pulse generator, and it seemed reasonable to extend that to checking the mercury tank driver circuit which comprise the last three valves on the chassis.

Thought was given to what potential damage might occur if power was applied and a cautious procedure was adopted to avoid any likely damage. The valve heaters are supplied from an on-board mains transformer, and damage to that would be particularly unfortunate. Careful inspection indicated that the transformer is in excellent condition externally with no signs of overheating. Resistance and insulation tests were also satisfactory. Mains power was applied to the transformer via a Variac, using croc-clips for connection so no soldering to the chassis was involved. Power was then very slowly increased over the course of an hour, with appropriate meters in circuit to look for any signs of trouble. This was carried out with no valves in place. The chassis as received had only one valve plugged in, and that had no connection pins on it. This initial test was most satisfactory as there was no sign of warmth after a further hour at full voltage but no load. The test was repeated with about half the valves in place, and again there was no sign of overheating or intermittence. It was concluded that the mains transformer was in excellent condition and would not be harmed by using it with a dozen valves in place. We do not have sufficient of the correct valves to fully populate the chassis.

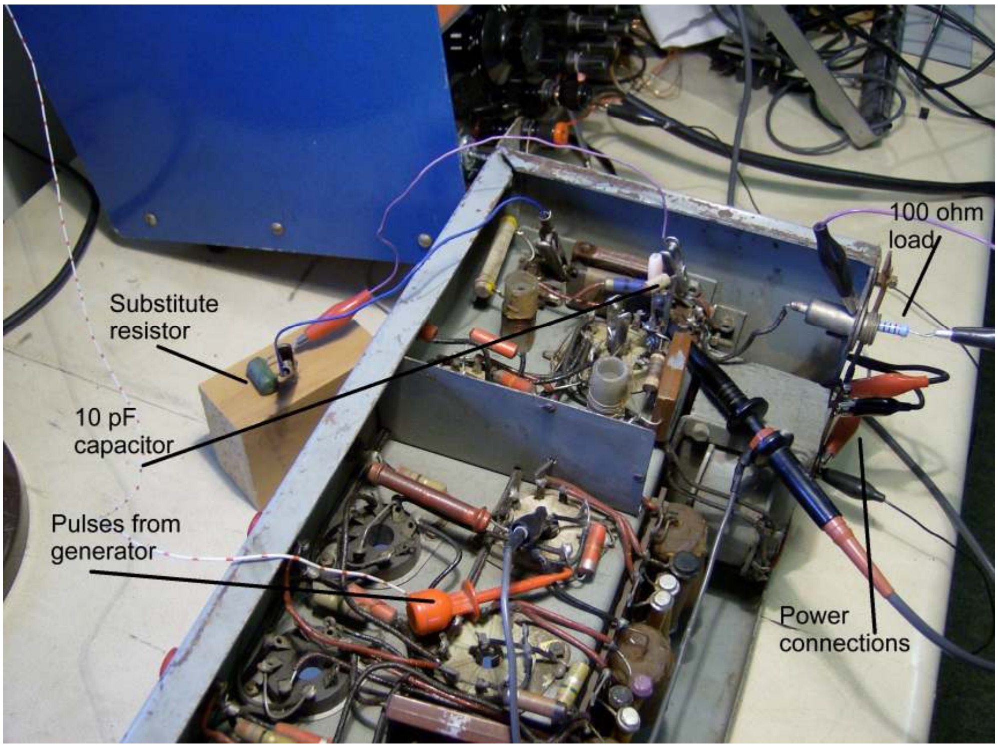
The second important test is to verify that no damage would be caused by applying the HT voltage of 250 volts, first with no valves and secondly with valves in place. With no valves in place we would expect a small current to flow in various voltage divider networks, and the numerous decoupling capacitors should charge up but not pass continuous current. A stabilised adjustable power supply was used and again connected to the chassis using croc-clips. With no valves in place, and no mains power on the heater transformer, the HT voltage was very slowly raised 50 volts at a time, with a ten minute pause at each step. The current remained exactly as expected, with negligible leakage through the capacitors. This is remarkable for such old components, perhaps indicating that they were originally over-specified to ensure reliability. The HT was left at 250 volts for half an hour, with no noticeable change in current. The voltage divider resistors correctly warmed-up. Next, the three tank driver valves V19, V20, V21 were plugged in, the heaters brought up to voltage on the Variac, and then the HT again brought up step-wise. Of course now there was significant current (about 45 mA) as the valves took current. The circuit was quiescent as there were no driving signals applied. It was noticed that there was no anode voltage on V21, traced to an open circuit resistor. A substitute resistor was connected across the faulty one, again using croc-clips to avoid any soldering operations for curatorial reasons.

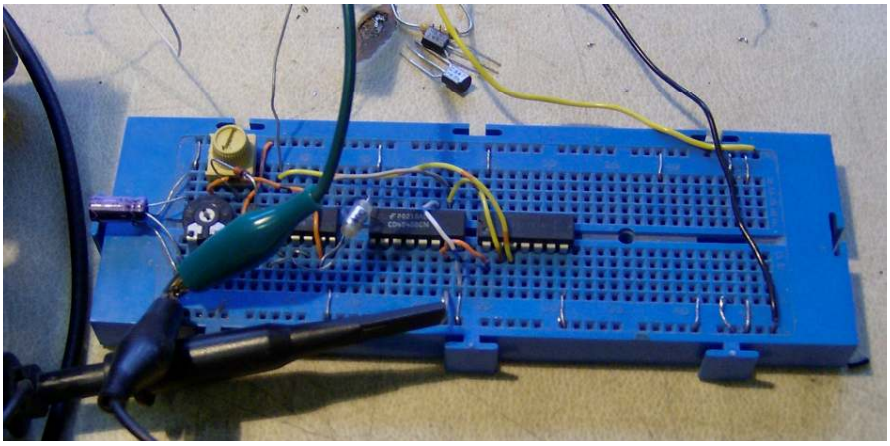
A mentioned above, an ad hoc chassis is already in use, wired up with various circuits including an AND-gate and an inverter which converts negative-going pulses to standard EDSAC positive-going pulses. This is being used to investigate some problems with the original circuit designs, which are somewhat less tolerant than we are familiar with nowadays. The source of signals is a breadboard of CMOS circuits set to provide clock pulses

0.9 µS wide occurring every 2 µS, which are the standard EDSAC timings. The pulse generator is arranged to provide two clock pulses every 8 µS. The valve inverter and a cathode follower then make standard 30 volt EDSAC signals. (For the time being we assume that is the standard size – awaiting more evidence from the documents and from experiments.) These double pulses were then connected to V19 input on the Regeneration Chassis. The HT power supply has to drive both the chassis and the ad hoc circuits and does not have sufficient current capacity for both, so this part of the experiment could only be done at 200 volts HT rather than 250 volts.

Reassuringly, the circuit worked, producing bursts of 13.5 MHz to correspond with each input pulse. The circuit diagram from the Wilkes and Renwick paper in *Electronic Engineering* shows a 10pF capacitor in the oscillator circuit, but there was no sign of that in the chassis. There is evidence of much past soldering in this area. A suitable capacitor was added using croc-clips, and it was possible to tune the circuit so the RF bursts were at the correct frequency. A 100 ohm resistor was inserted in the output socket to represent the impedance of the cable and quartz crystal in the mercury tank.

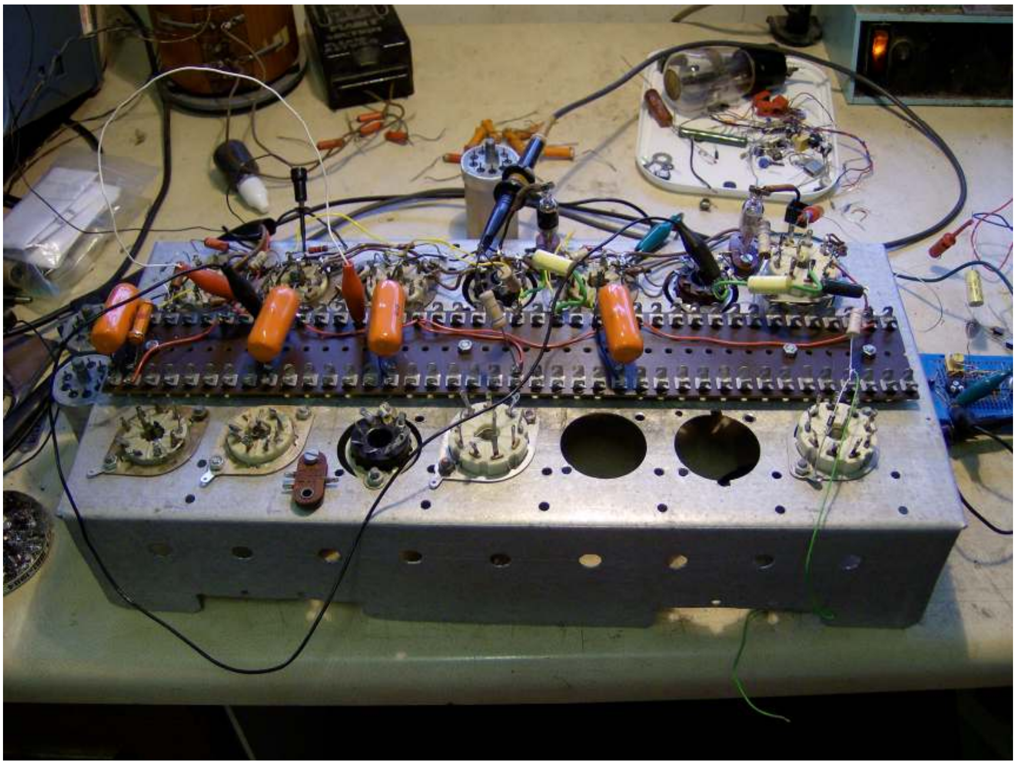
The tank driver circuit at the end of the chassis.

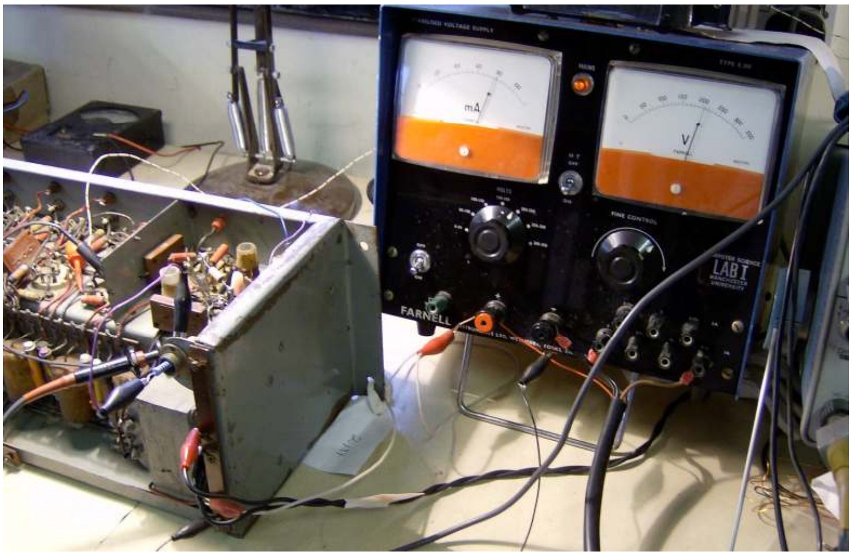




Breadboard with clock pulse generator and waveforms source

Experimental unit with AND-gate, cathode followers, inverter etc. Used here to turn CMOS pulses into EDSAC signals.



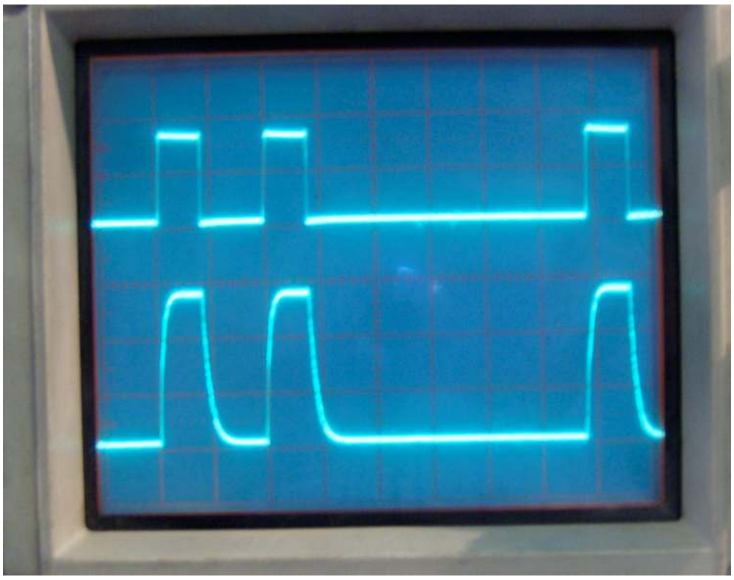


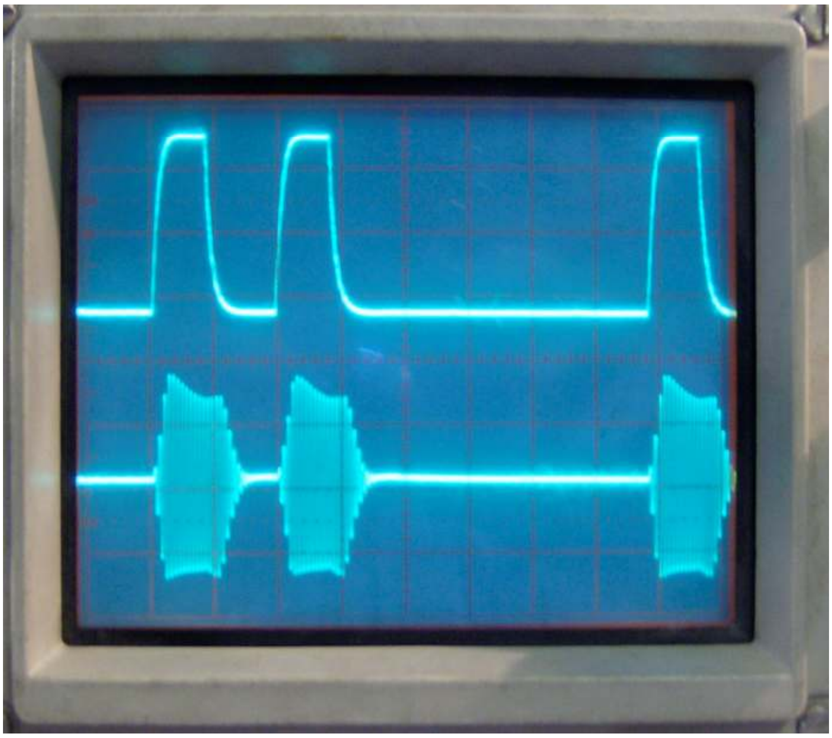
HT power supply operating at 200 volts instead of nominal 250 volts, due to its internal current limiter.

Top trace – CMOS pulses 17 volts high.

1 μS per division.

Lower trace – “EDSAC” pulses 30 volts high. Note slow edges with this valve technology at these speeds.





Top trace – “EDSAC” pulses.

1 μS per division

Lower trace – 13.5 MHz bursts to tank quartz crystal. Amplitude 30 volts p.p.

Top trace – clearer view of the RF burst to the tank.

0.5 μS per division